Plenty of Reasons to Be Confident About EUV Lithography

Vivek Bakshi, EUV Litho, Inc.
March 11, 2009

It was standing room only during the extreme ultraviolet lithography (EUVL) sessions at this year's SPIE Advanced Lithography conference, which caused me to do some quick math as I clung possessively to my seat. With conference attendance reportedly down 50% from last year but the EUVL meeting room as packed as it was last year, I could only conclude that the industry's interest in this branch of lithography had doubled. Fortunately, the packed-in attendees got what they had hoped to see — defectivity and yield data on process development and tool performance that appears to show that EUVL continues to make progress in meeting high-volume manufacturing (HVM) requirements.

In my opinion, the reported progress on EUVL was awesome. Accounts from some other observers at the conference reported a lack of progress in resist, mask and sources for EUVL, making me wonder if they had attended the same conference as I had — or maybe had skipped over some of the major papers. For that reason, I'd like to offer a more optimistic assessment of EUVL's future.

Scanners

The EUV session started Tuesday morning with a keynote presentation by ASML on the status of its EUVL scanner program. The uptime of the company's alpha demo tool (ADT) vacuum system is now >95%. With an updated tin discharge-produced plasma (DPP) source, the current throughput of 4 wph will increase to 6 wph for 5 mJ resist. I think tin DPP sources will improve much more to deliver even greater throughput this year (see "Source development," below). Single-tool overlay is now at 4 nm.

ASML presented process data at 28 nm half-pitch for 1:1 lines and spaces (L/S) with &10% critical dimension uniformity (CDU). Presenters also showed a large process window (>200 nm for 28 nm L/S) for EUVL compared with ArF immersion, which is why the industry continues to stand behind EUVL. Optics quality has steadily improved, with peak reflectivity of 69.6% compared with 64.5% in the ADT, which will allow 50% higher transmission.

Nikon also showed process development results from its alpha tool, EUV1, which is now performing dynamic exposure (although not yet at full speed) for 40 nm hp with 5 nm line-edge roughness (LER) and CDU of 2.4 nm (3σ) at the center. Nikon is working on fly-eye mirror optics to minimize transmission loss for its next-generation scanner. Flare is still high at 14%, but I was surprised to hear that a spectral purity filter (SPF) has no effect on flare numbers.

I also read speculation in some recent press coverage about $90M EUVL tools. Of course, I cannot predict what manufacturing-ready EUVL tools will cost, but credible discussion on this point must be based on cost of ownership (CoO). ASML, which dominates this particular scanner market, will happily sell you two 193

nm immersion scanners for double pattering instead of one EUVL scanner. But its own CoO calculations, shown in the keynote talk, concluded that end users will realize significant cost savings from EUVL compared with immersion/double patterning at 22 nm. This should put an end to the debate on whether the cost of EUVL will be competitive with that of double patterning. ASML's CoO calculations conclude that end users will realize significant cost savings from EUVL compared with immersion/double patterning at 22 nm.

Process development results

In another keynote talk, AMD showed its process development results for the 22 nm node (although AMD in 2008 showed process development results for the 45 nm node, its researchers and partners in the IBM Alliance skipped over 32 nm because they expect EUVL implementation to occur beyond 22 nm). The company's process development was done on highk1 imaging with conventional optical proximity correction (OPC), single exposure, and no forbidden pitches or restricted design rules.

Like other manufacturers, AMD insisted on seeing actual measured source power at first focus as a sign of progress for sources. Other end users presented data on flare estimation, process integration, yield and defects — reassuring participants that full process development for implementing EUVL at 22 nm is well underway.

Source development

EUV sources have made good progress, but still are the main obstacle to high-volume chipmaking goals. A little history might be useful to fully understand the issues here, starting with sources based on laser-produced plasma (LPP). The EUV LLC consortium (1997-2002) produced the most recent reliable LPP source for printing circuits, using xenon as fuel to generate about 1 W of power. These results were encouraging enough for the industry to start investing in commercial EUVL tools for HVM.

Fast-forwarding to the present, ASML's roadmap calls for a 100 W tin LPP source for beta-level scanners (while Nikon is looking at both DPP- and LPP-based sources for HVM). ASML's plan is a leap of two orders of magnitude from the last time we saw a working LPP source. It also supplants xenon with tin, which is a harder material to deliver and mitigate. Also, we have not even demonstrated that a 10 W LPP source with a 100% duty cycle and a fully integrated collector is even feasible — and a 100 W goal is even further away. I believe we need more realistic goals, such as 25-50 W, to gain user confidence.

However, tin LPP has made impressive progress in many areas: large, high-temperature collectors with peak reflectivity of 65%, tin delivery system with 10 μm droplets, and pulsed high-power CO_2 lasers. If we can develop a 25 W source at 100% duty cycle, fully integrated with a collector module, we'll go a long way in convincing the industry of EUVL's feasibility. Anyone for inserting this new target into the roadmap?

Although 45 W burst-mode data was presented for tin LPP sources, it was based on power measurements at source, which were interpolated to estimated power at first focus under assumptions of a 5 sr collector and 90% transmission. This did not convince me that 100 W power from tin LPP is coming anytime soon.

Even though an 18× improvement in integrated system performance was claimed, I could not figure out from the talks where LPP source power is today, so that we can compare it with current DPP performance. To do this, we need data from an integrated source collector module (SoCoMo), measuring at first focus with 100% duty cycle. When source experts like me cannot figure out the performance data, I wonder how many others in this industry can understand the true status of tin LPP.

I don't mean to say that tin LPP is not doing well — both Cymer and Gigaphoton have made large investments and continue to work hard toward progress in this technology. Gigaphoton presented four-hour continuous operation data (2.5% duty cycle, 5 kW CO_2 laser, with conversion efficiency of 1.5%). If such a run can be done at 100% duty cycle and one-third of source power can be collected, then 25 W can be obtained at first focus. Of course, integrated system performance still needs to be demonstrated.

Today, tin DPP sources are at 10 W levels. The theoretical efficiency of tin is in the 7-8% range, but only 2% or less has been achieved so far. In the conference, Philips Extreme UV researchers showed that they have doubled the conversion efficiency of their tin DPP source. This is good news: For the same heat load, debris and out-of-band radiation, you can get twice the number of EUV photons. A lot of research has been done on using clever tricks to obtain higher conversion efficiency for tin LPP, and I hope tin DPP can benefit from that.

ASML's roadmap looks good, except for its dependence on LPP technology only. The company also showed data on a 100% duty cycle for a 350 W tin DPP source for one hour (power was measured at the source, which at current 6% collection efficiency translates to 21 W at first focus). I have a feeling that no one can afford to bypass a working technology, and so if 25 -50 W fully integrated tin DPP sources become available, they will show up in beta scanners.

Resist

LER status received much attention, with Patrick Naulleau of Lawrence Berkeley National Laboratory (LBNL) presenting one of the most interesting papers of the conference. He has taken total measured resist LER and separated out contributions from masks, showing that masks contribute a big factor in the measured LER in resists.

Nalleau's best LER measurements have been at 2.1 nm for 17 mJ resist. His experiments allowed him to predict a mask contribution of 1.43 nm, which indicates that the best LER result to date is 1.5 nm. Not bad, especially combined with a report by ASML (using results from Intel process development) that for an 8.7 mJ resist, LER can be reduced from 5.3 nm to 3.9 nm (a 26% reduction) via a selection of pre- and post-rinse agents.

What really matters is the LER in the final etched features, and I did some work almost 10 years ago to demonstrate how selection of etch recipes can help reduce transfer of resist LER to the LER of final etched features. So while resists continue to improve, a combination of reduced mask-induced LER, innovative rinse agents, and etch chemistries can get LER under control.

ASML showed data for 10 mJ resists that are on target to satisfying resolution requirements for the 27/22 nm node (LWR 10% of resolution). The improvement in EUV resists is impressive but not very

surprising, since they are being developed by well established suppliers with a good understanding of resist chemistry.

Masks

Mask defects continue to get attention as the leading challenge. One reason is that requirements for mask substrates are zero defects at >50 nm defect size, and for mask blanks zero defects at >30 nm. For substrates, pit defects remain the dominant type. A Sematech paper by Abbas Rastegar showed that we can now clean particles >30 nm. Pits, with dimensions averaging ~9 nm deep and 100 nm wide, must be cleaned via smoothing.

The results of etch approaches to reduce the printability of pit defects also were shown. Interestingly, pits with an aspect ratio &0.1 and depth &2.4 nm will not print. I predict that substrate defects will be addressed via pit smoothing, and mask blanks will be fixed by ion-beam repair and defect compensation in mask writing.

At this point, we should also consider the latest results on defect printability. It was shown that defects >60% of half-pitch will print. At 32 nm hp, defects will print if they are 21 nm on wafer and 84 nm on the mask. This is clearly more relaxed than the current defect requirements. It may be the reason for AMD reporting that in its 22 nm hp development, the researchers expected to see defect printability of 11-23/cm2, but only 1-3/cm2 actually printed on devices.

There has been tremendous improvement in reducing the number of defects added during handling, with current data from Nikon showing one to seven defects added per cycle at 55 nm.

Defect inspection

Further improvement in defect reduction will come as actinic inspection tools (aerial image measurement system [AIMS] and full blank inspection) become commercially and readily available. Intel noted that the lack of commercial tools for actinic inspection is one of the leading unfunded challenges for EUVL, with a $150M investment required to enable production of commercial tools.

MIRAI presented results from its actinic mask blank inspection tool, which can detect 60 × 1.5 nm bumps and 120 × 2.3 nm pits. At this inspection specification, it has an 80% capture rate and a 100% rate for larger defects, and can inspect a blank in 2-10 hours. The tool is powered by a xenon DPP EUV source from Energetiq. Because an actinic inspection source has a very small numerical aperture (NA — 0.1, in this case) and hence uses a very small part of source power, sources with higher brightness will be needed to increase inspection speed. Given that the industry has not quite decided on specifications, the 2009 International Workshop on EUVL taking place in Honolulu in July will convene an actinic inspection panel to generate consensus on technology requirements.

OPC

As EUV light is incident on the masks at 6¢ª, it results in different bias for horizontal and vertical lines (H-V bias). Looking to correct this effect and compensate for flare, many papers were presented on OPC for EUV. Since OPC requirements are much simpler for EUV than for extended 193 nm lithography, I believe there are enough experts in the industry to adequately address this challenge.

Predictions

Just as a new theory in physics has to make verifiable observations, so must an industry analysis also be put to the test. So stepping up to that challenge, I will make a few predictions:

Tin DPP power will double in 2009 (100% duty cycle for an integrated source). Tin LPP will make significant progress, but will not deliver a 100 W integrated source in 2009.

Masks will not reach their zero defect targets, but a combination of defect reduction and repair techniques will meet productivity goals for the 22 nm node.

Resists will not meet current LER goals, but the process goals for LER will be reached via reduced mask contribution to LER and improvements in etch chemistries, including innovative rinse techniques.

Optical contamination, OPC and reticle handling defect requirements will be dealt with satisfactorily.

Final comments

During the conference, I heard that Litho Guru and Gentleman Scientist, Chris Mack, was predicting the demise of EUVL in two years. He provided a very clear indicator for verifying his predictions (unlike some of the performance results for EUV sources presented at the conference), so his position has to be respected. His indicator is this: “Number of submitted abstracts in the area of EUVL for 2011 SPIE Advanced Lithography conference will be zero.”

In diametric opposition, I predict the implementation of EUVL in fabs by the 2013-14 timeframe, or earlier. So, Chris and I have bet a Lotus sports car on who will be right. I am so sure of my prediction that I have already ordered my custom license plate, “EUVL,” while I await the delivery of my new car.